BSc Physics (V Semester) - Assignment

1. Convert the following numbes to binary (i) 25 (ii) -35 (iii) 23.56 (iv) $2.8x10^8$
2. A digital system uses a 40 bit system for representing floating point numbers in which 16 bits are used for exponent and 24 bits for mantissa. Calculate the accuracy and range possible for this system
3. Perform the following arithmetic operation in 2's complement binary (a) 4-(22) (b) 38-(-21)
4. Draw the logic circuit for Y= (A + B + C)(A + B + C). Use Boolean algebra to simplify the equation. Then draw the corresponding logic circuit.
5. A logic circuit with 4 input should give a high output for inputs 0,1,2,3,4,5,6,7,8,9 and 10. Obtain the simplest circuit using Karnaugh mapping.
6. A transmitter radiates a power of 1000W. When it is modulated with a modulation factor of 50%, calculate the power in each side band.
7. An audio signal of 1kHz is used to modulate a carrier of 500kHz as amplitude modulated wave. Determine the sideband frequencies and bandwidth required.
8. A full wave bridge rectifier has a load of 3.5 kΩ. If the forward resistance of each diode is 4 Ω and the input voltage has a peak value of 300V, Calculate (i) peak, average and rms value of current flowing. (ii) dc power output (iii) ac power input (iV) efficiency of the rectifier.
9. A volatge regulator using zener diode has the following components. Series limiting resistance R=2.2 kΩ, load resistance R_L=10 kΩ and xener volatge Vz=15V. If the input voltage varies between 20-30V calculate the maximum and minimum current through the zener diode. Also calculate the power dissipated in zener diode in each case.
10. An op-amp circuit in non-inverting configuration has R_I=2.2 kΩ and R_F=22 kΩ. Calculate the maximum input that can be given with out the output being saturated. What would be the output for the same input when the configuration is changed to a inverting amplifier with same component values. Assume the power supply is of ±12V.
11. An op-amp integrator has a resistance of 10 kΩ and capacitance of 2.2μF. If the power supply is of ±12V, calulate the time taken for the output to get saturated.
12. The drain resistance and transconducatnce of a FET are to determined experimentally. The following observations have been noted. With V_{GS}=0 and V_{DS}=7V the drain current is 10mA. When the drain voltage is increased to 15V keeping V_{GS} constant the drain current increases to 10.25mA. When V_{GS} is changed to -0.2V while keeping V_{DS} at constant 15 V, the drain current reduces to 9.6mA.

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